Optically Induced Measurement Anomalies with Voltage-Tunable Analog-Control MMIC's

Stepan Lucyszyn, *Member, IEEE,* and Ian D. Robertson

Abstract—**Monolithic microwave integrated circuits (MMIC's) may be measured under relatively high-intensity lighting conditions. Later, when they are packaged, any anomalies found in subsequent measurements could be attributed to unwanted parasitics or box modes associated with the packaging. However, optical effects may not always be considered by radio-frequency (RF) and microwave engineers. For the first time, a qualitative assessment is given for the effects of photonic absorption on three broad-band voltage-tunable analog-control circuits. Each circuit has a different function, with each field-effect transistor (FET) operating in a different mode: a hot FET in a variable-gain amplifier, a cold FET in an analog attenuator, and an FET varactor in an analog phase shifter. All three circuit functions have been implemented using two different FET-based technologies. The first with ion-implanted 0.5-μm GaAs metal–semiconductor FET's (MESFET's) in circuits operating at either 3 or 10 GHz. The second employs epitaxially grown 0.25-μm AlGaAs/InGaAs pseudomorphic high electron-mobility transistors (HEMT's) in circuits operating at 38 GHz. All the MMIC's were fabricated using commercial foundry processes and illuminated under conventional optical microscope lighting conditions. Prominent error peaks have been found at bias points unique to the three different circuit topologies. Large error peaks are found with the MESFET-based circuits, while much smaller error peaks are achieved with the corresponding pseudomorphic HEMT (pHEMT) based circuits.**

Index Terms—**Analog control, optoelectronic, MMIC.**

I. INTRODUCTION

MONOLITHIC microwave integrated circuits (MMIC's) have a number of important advantages over the more traditional hybrid microwave integrated circuits (HMIC's) [1]. With the falling costs associated with on-wafer radio-frequency (RF) measurements fueled by the rapid rise in demand, an ever increasing number of MMIC design groups are establishing their own in-house MMIC test facilities.

With the extremely high levels of mechanical precision found in today's measurement equipment, and the corresponding advances in their calibration procedures, MMIC's can be measured to very high levels of accuracy—to at least three decimal places in both magnitude and phase, well into the millimetric frequency range. MMIC's are measured using either test fixtures or on-wafer probing techniques [1], [2]. With the former, the MMIC is measured under ambient laboratory lighting conditions, using fluorescent tubing, and perhaps with an additional tungsten fila-

ment spot lamp. However, with on-wafer probing, the miniature probe tips must be accurately placed onto the MMIC's probe pads with the aid of an optical microscope and an additional high-intensity light source. Often, engineers with limited experience in measuring MMIC's perform both the initial probe alignment and subsequent measurement procedures under the same lighting condition. Later, when the MMIC is either individually packaged or incorporated into a more complex HMIC, any anomalies found in the subsequent measurements could be attributed to unwanted parasitics or box modes associated with the packaging. However, optical effects may not always be considered by RF and microwave engineers.

Precision control circuits play an important role in general adaptive signal-processing applications. When compared to purely digital implementations, analog-control circuits offer considerable advantages [3]. As a result, analog-control circuits appear ideal for large adaptive phased arrays [4] and adaptive multifunction MMIC designs. For example, the adaptive phased-array antenna, employing control circuits such as variable attenuators and variable phase shifters [4], is the single most important application of MMIC's for space and portable radar systems. Unfortunately, voltage-tunable analog-control MMIC's are particularly susceptible to measurement anomalies due to photonic absorption because they have to operate over wide bias voltage ranges. However, little information has been reported to quantify the optical effects on real analog-control circuits having different functions and with different field-effect transistor (FET) based technologies operating in different modes.

Based on an extensive experimental study, this paper gives a qualitative assessment of the effects of photonic absorption, during on-wafer RF measurement, for three broad-band voltage-tunable analog-control circuits. Each circuit has the following different function, with each FET operating in a different mode:

1) hot FET in a variable-gain amplifier;
2) cold FET in an analog attenuator;
3) FET varactor in an analog phase shifter.

All three circuit functions have been implemented using two different FET-based technologies. All the MMIC's were fabricated at GEC-Marconi Material Technology Ltd. (GMMT), Caswell, U.K., using their standard commercial foundry processes. Since GMMT is one of Europe's largest vendors of GaAs MMIC's, the results from this study will be highly relevant to those involved in the design and measurement of voltage-tunable analog-control MMIC's.

II. PRINCIPLE MECHANISMS

Optically controlled microwave devices and circuits have been studied for many years [5]–[9]. They have been deployed in many diverse applications, including optical phase-lock loops [10], optical injection locking of microwave oscillators [8], [11], and adaptive phased-array antennas, [10], [12]. The effects associated with optically illuminating FET's are well understood [13]–[17]. A brief summary of the three principle effects will be described in this section.

When a device is illuminated by a light source, whereby the photon energy is equal to or greater than the band-gap energy, the absorbed photons initially generate a plasma of free-charge carriers (electron–hole pairs) in the section of exposed semiconductor. Since the carrier recombination time is greater than the transit time across the depletion region or undepleted channel, these excess carriers result in photoconductive and photovoltaic effects. If the optical illumination intensifies or the FET's peripheral size increases, the number of electron–hole pairs increase and the observed photoconductive and photovoltaic effects become more pronounced.

A. Photoconductive Effect

In the undepleted region of a doped semiconductor, any excess carriers will increase the real part of the complex relative permittivity and, therefore, the associated intrinsic parasitic capacitances increase in value. However, the resulting effects may only become significant at millimeter-wave frequencies. The imaginary part of the complex relative permittivity is also increased. As a result, the effective conductivities in this region increase and, therefore, the associated intrinsic parasitic resistances decrease in value, which may have noticeable effects at any frequency.

If a drain–source voltage is applied to the FET, the resulting electric field across the neutral channel (underneath the gate electrode) will cause the electron–hole pairs to separate. The resulting photoconductive current will be in addition to the normal drain current. This optically induced excess drain current will be less than a microampere with FET's that have short gate lengths.

B. Internal Photovoltaic Effect

When epitaxial growth techniques are used to create the active layer (epilayer) there is an abrupt change in the doping concentration profile between the n-type channel and the buffer/substrate. As with p-n junctions, a depletion region is formed due to the difference in doping levels (several orders of magnitude). In the illuminated sections of this interfacial depletion region, the associated electric field will cause the electron–hole pairs to separate. Since this photocurrent flows via the high-resistivity buffer/substrate, a photovoltage is induced across the buffer/substrate, which opposes the natural built-in barrier potential across the interfacial depletion region. As a result, the interfacial depletion region will shrink in the illuminated sections, increasing the height of the channel and, thus, increasing the drain current flow. This optically induced excess drain current can be in the order of milliamperes.

C. External Photovoltaic Effect

In the exposed section of the gate's Schottky-junction depletion region, the high associated electric field will cause the electron–hole pairs to separate, creating a gate photocurrent. Also, electron–hole pairs generated in the channel can contribute to this gate photocurrent by diffusing into the gate's depletion region before recombination can take place. The combined gate photocurrent will flow out of the gate electrode and through the gate bias resistor. As a result, a photovoltage is induced across the gate bias resistor, which superimposes itself onto any externally applied reverse-bias gate voltage. However, this photovoltage effectively tries to forward bias the gate junction. Therefore, the gate's depletion region will shrink, increasing the height of the channel and, thus, increasing the drain current. This optically induced excess drain current can be in the order of tens of milliamperes. If the gate bias resistance is large enough, the small gate photocurrent will be large enough to produce a photovoltage that could completely cancel out the externally applied gate bias.

III. FET TECHNOLOGIES AND MEASUREMENT SETUP

The MMIC's were fabricated using GMMT's standard F20 commercial foundry process, which is based on ion-implanted 0.5-μm GaAs metal–semiconductor FET's (MESFET's) and mesa-etched resistors. The cross section of the F20 MESFET's gate region is illustrated in Fig. 1(a). With this process, there is no buffer layer between the channel and substrate and, therefore, these MESFET's should not suffer from internal photovoltaic effects. The semi-insulating substrate is first silicon doped ($\sim$3 $\times$ 10^{17} cm^{-3}) to form the n channel, using high energy ion implantation—which leaves a Gaussian doping concentration profile. This is then followed by a second silicon doping ($\sim$2 $\times$ 10^{18} cm^{-3}) at a lower energy to form the n$^+$ capping layer. The trapezoidal gate MESFET has a single recess structure.

The monolithic millimeter-wave integrated circuits were fabricated using GMMT's standard H40 process, which is based on epitaxially grown 0.25-μm Al$_{0.23}$Ga$_{0.77}$As/ In$_{0.15}$Ga$_{0.85}$As pseudomorphic HEMT's (pHEMT's) and nichrome resistors [18]. The cross section of the H40 pHEMT's gate region is shown in Fig. 1(b). These pHEMT's may suffer from internal photovoltaic effects because there is a buffer layer between the channel and the substrate. A 150-Å-thick undoped pseudomorphic InGaAs channel is first grown by molecular beam epitaxy (MBE) onto the undoped GaAs buffer layer. A 20-Å-thick undoped AlGaAs spacer layer and a 300-Å-thick silicon doped (2.0 $\times$ 10^{18} cm^{-3}) AlGaAs supply layer are then grown. Finally, a 500-Å-thick silicon doped (2.5 $\times$ 10^{18} cm^{-3}) capping layer is grown, which serves to optimize the formation of ohmic contacts. The mushroom gate pHEMT has a double-recess structure. The outer recess is etched into the capping layer without exposing the supply layer.

The MMIC's were first measured using conventional on-wafer RF probing techniques, while being illuminated under broad-band white light conditions. The commercial microscope light source used (Techni-quip) consists of a standard
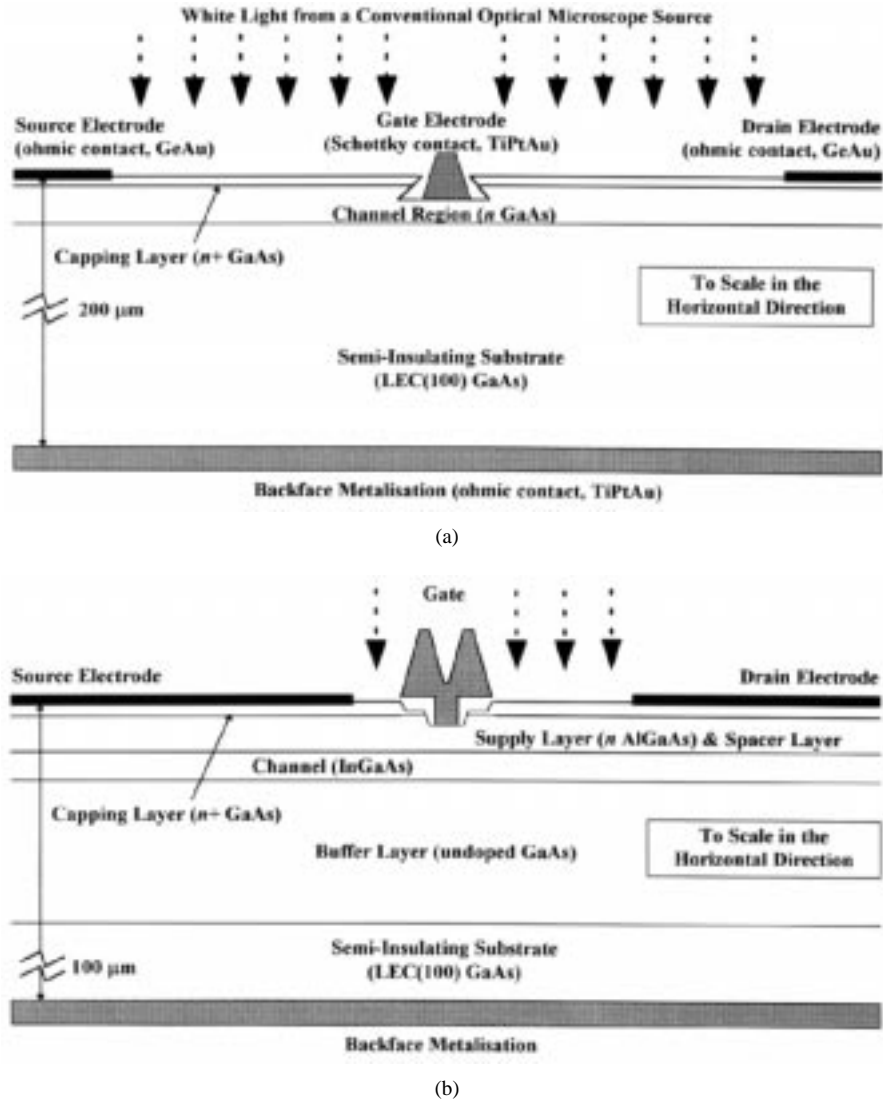
Fig. 1.   Illustration of the FET's cross section at the gate region. (a) MESFET. (b) pHEMT.

150-W halogen bulb with a short fiber-optic cable feeding a 65-mm-diameter slit-ring aperture, which was placed 70 mm above the MMIC-under-test. The MMIC's were then measured with no illumination to emulate the ambient lighting condition of a packaged chip.

The MMIC's were designed to act as either variable-gain control blocks or variable-phase control blocks. Only one externally applied control voltage was required for each circuit. A single-gate bias resistor was employed to prevent RF leakage and to act as a forward-bias current limiter. The value of this resistance must be high enough to prevent RF leakage. However, if the resistance is too high, the switching speed of the circuit my be compromised and the external photovoltaic effect may cause significant measurement anomalies. With the MESFET-based MMIC's, the value of gate bias resistance was 6 kΩ. This value is more than ample for achieving good RF isolation, but not too large so as to induce a significant photovoltage of its own. However, it will be seen that these MMIC's suffer from significant anomalous measurements due to the external photovoltaic effect. With the pHEMT-based MMIC's, the value of bias resistance was chosen to be

either 750 or 375 Ω. As a result, the observed anomalous measurements due to the external photovoltaic effect are greatly reduced.

IV. VARIABLE-GAIN AMPLIFIERS

Active variable-gain blocks are used extensively in communication subsystems. For example, they can be used for implementing digital modulation performed directly at carrier frequency (including M-ASK and M-QAM). Other examples include automatic gain controls [19] and providing positively weighted taps in direct implementation adaptive microwave signal-processing applications.

A. MESFET-Based Amplifier

The topology and corresponding microphotograph of the MMIC variable-gain amplifier are shown in Fig. 2(a) and (b), respectively [19]. The amplifier employs a single 400-μm MESFET, with the drain voltage fixed at $V_{\text{dd}} = +5$ V. Tuning is achieved by simply varying the gate bias voltage. The resulting tuning curves under both lighting extremes are shown in Fig 3(a). It can be seen that this amplifier achieves a
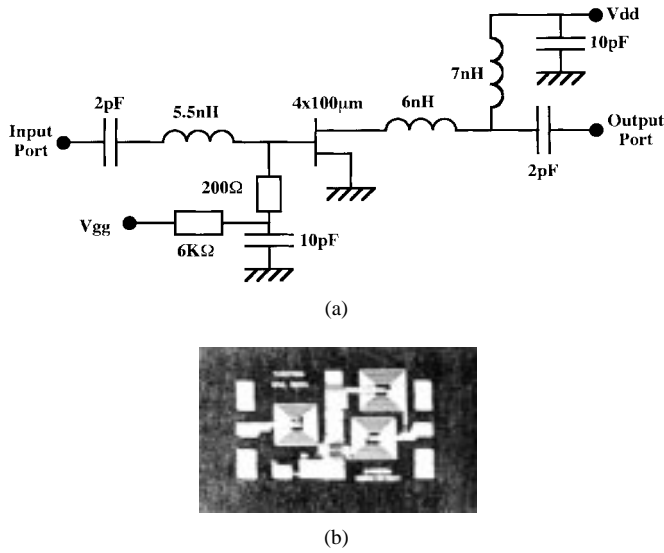
Fig. 2. Microwave variable-gain amplifier. (a) Topology. (b) Microphotograph.

dynamic-tuning range of almost 30 dB, at the center frequency of 3 GHz.

With a hot MESFET, the intrinsic transconductance increases with increased illumination, due to both the photoconductive and photovoltaic effects. The resulting bias-dependent measurement-error characteristic (i.e., the difference in insertion gain responses) is also shown in Fig. 3(a). It can seen that a 5.5-dB error peak is located at a negative-gate bias potential of 1.95 V. As would be expected, this corresponds to the nominal device pinchoff voltage of $V_{\text{pinchoff}} = 2.0$ V. When deployed as a variable-gain single-stage amplifier, a 5.5-dB drop in the expected level of power gain could have dramatic consequences when integrated into a system. As a fixed-gain Class-A amplifier biased for maximum gain or maximum linearity, this error characteristic is of little concern since the gate would be biased well away from pinchoff. However, as a fixed-gain Class-B power amplifier, this error characteristic is of great importance since the gate is biased at pinchoff. Problems may also be found with Class-A/B amplifiers.

B. pHEMT-Based Amplifier

The topology of the millimeter-wave variable-gain amplifier is similar to the microwave amplifier, except that feedback has been added and distributed transmission lines have replaced the lumped-element matching circuitry. The amplifier employs a single 120-μm pHEMT, with the drain voltage fixed at $V_{\text{dd}} = +2$ V. The resulting tuning curve under both lighting extremes are shown in Fig 3(b). It can be seen that this amplifier achieves a dynamic-tuning range of only 10 dB, at the center frequency of 38 GHz.

The resulting bias-dependent measurement-error characteristic is shown in Fig. 3(b). It can seen that the very small 0.7-dB error peak is located at a negative-gate bias potential of 0.9 V. Again, the location of this peak corresponds to the nominal device pinchoff voltage of $V_{\text{pinchoff}} = 0.9$ V. Therefore, if the hot pHEMT is employed in a low-noise
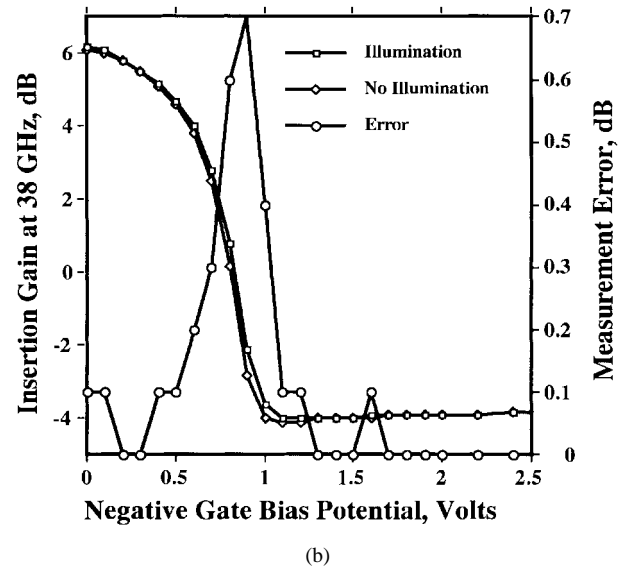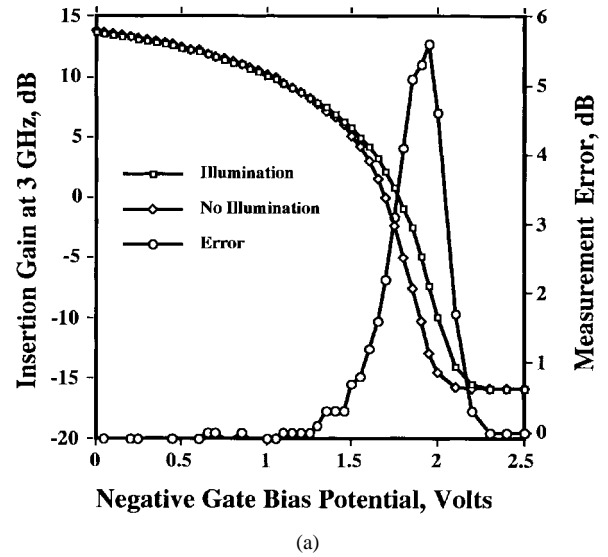

Fig. 3. Measured anomalous optical behavior for the variable-gain amplifier. (a) MESFET circuit. (b) pHEMT circuit.

amplifier, where its gate bias is set close to pinchoff, then anomalous measurements will be observed.

It should be apparent that with variable-gain amplifiers the error peak will always be found at pinchoff, irrespective of the FET's peripheral size or the frequency of operation. However, the size of the error peak will depend on the FET technology used. Moreover, the peripheral size of the FET tends to be inversely proportional to frequency when operating near its cutoff frequency ($f_T = g_m/2\pi C_{\text{gs}}$) because the value of gate–source capacitance C_{gs} is proportional to the peripheral size. As a result, at higher frequencies of operation, the FET's become smaller and, therefore, the size of error peaks become smaller.

V. ANALOG ATTENUATORS

A biphase analog amplitude modulator is a special case of a variable-gain block [1], [3]–[4], [20]. In principle, it can be used as a variable attenuator in either of two phases
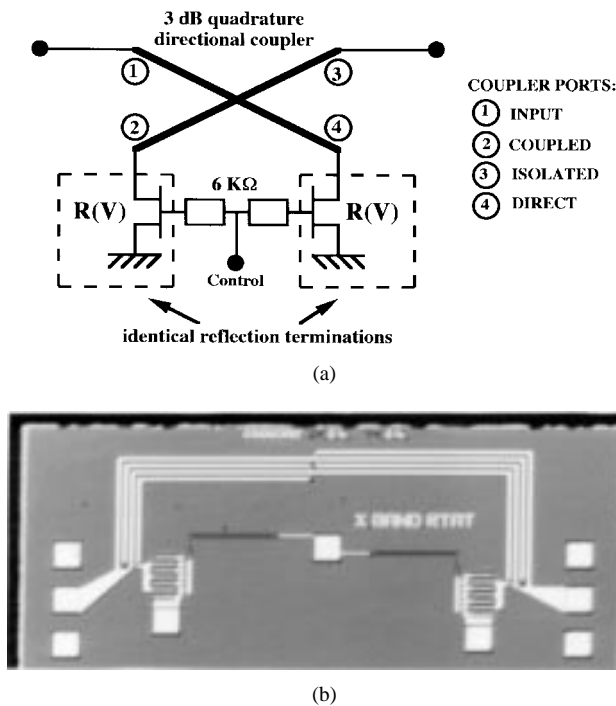
Fig. 4. Microwave analog attenuator. (a) Topology. (b) Microphotograph.

and, therefore, it can be employed in all of the applications listed previously for the variable-gain amplifier [21]. In addition, biphase modulators are used to implement elegant binary phase-shift keying (BPSK) modulator designs and in-phase–quadrature phase (I–Q) vector modulators [20], [22].

A. MESFET-Based Attenuator

The topology of a microwave biphase modulator is shown in Fig. 4(a). This reflection topology consists of a 3-dB quadrature directional coupler with two identical cold MESFET's, which act as voltage-controlled variable-resistance reflection terminations. This reflection topology can be effectively treated as a single-MESFET circuit because of the inherent characteristics of the directional coupler. With no gate bias voltage applied, the drain–source channel resistance should ideally be a short circuit and the insertion loss will be at its minimum level. As the negative-gate bias potential increases, so too will the channel resistance and, as a result, the insertion loss will increase. When the termination resistance is equal to the reference impedance of the coupler (e.g., 50 Ω) the insertion loss should theoretically, approach infinity. As the negative-gate bias potential and the corresponding channel resistance increase further, the insertion loss decreases. At pinchoff, the termination resistance should ideally approach an open circuit and the insertion loss is once more at its minimum level.

Cold MESFET's have been accurately characterized at microwave frequencies [23] and subsequently deployed in numerous MMIC applications ranging from reflection topology building blocks for adaptive microwave signal-processing applications [3] (including variable beam-forming networks [4] to tunable active inductors used in tunable active bandpass filters [24] and tunable notch filters [25]).
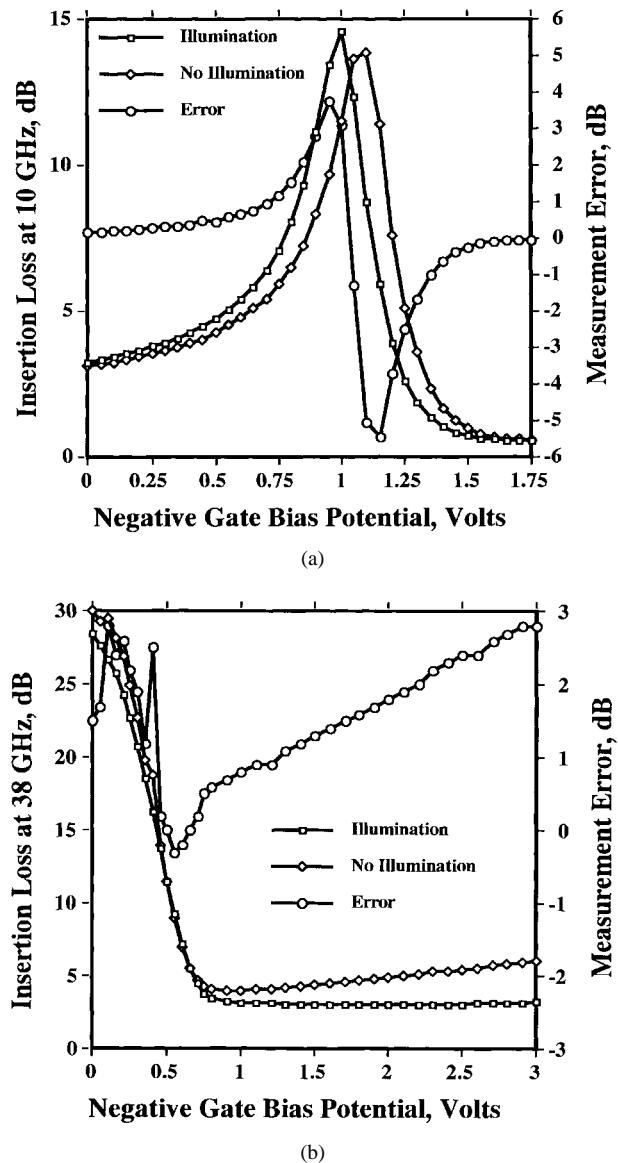

Fig. 5. Measured anomalous optical behavior for the analog attenuator. (a) MESFET circuit. (b) pHEMT circuit.

A microphotograph of the MMIC biphase modulator is shown in Fig. 4(b) [3]. The circuit employs 600-μm MESFET's, with the drain voltage fixed at $V_{dd} = 0$ V. Tuning is achieved by simply varying the gate bias voltage. The resulting tuning curves under both lighting extremes are shown in Fig. 5(a). It can be seen that the modulator achieves a dynamic-tuning range of almost 15 dB at the center frequency of 10 GHz.

With cold MESFET's, the drain–source channel resistance decreases with increased illumination due to both the photoconductive and photovoltaic effects. The resulting bias-dependent measurement-error characteristic is shown in Fig. 5(a). It can seen that there are two error peaks located at 0.95 and 1.15 V. The first peak is just below the gate potential that causes the channel resistance with no illumination to equal 50 Ω, while the second peak is just above the potential that causes the channel resistance to equal 50 Ω when illuminated. When deployed as a single-stage analog attenuator, a worst-

case error of 5.5 dB in the expected level of insertion loss could have dramatic consequences.

B. pHEMT-Based Attenuator

The millimeter-wave analog attenuator is similar to the microwave attenuator (but with a 750-Ω gate bias resistor), except that now two biphase modulators are configured in a balanced topology having a push–pull mode of operation [26]. The result is an attenuator that can achieve a much larger dynamic-tuning range. For simplicity, one of the biphase modulators has been deactivated by disconnecting its control line. When a zero-gate bias voltage is applied to the active modulator, the signals emerging from both arms of the balanced topology are inherently of equal magnitude and 180° out-of-phase, thus providing a high level of insertion loss (due to complete signal cancellation). When the gate bias voltage is set at pinchoff, the emerging signals are ideally of equal magnitude and in-phase, thus providing the minimum level of insertion loss.

The attenuator employs 240-μm pHEMT's, with their drain voltages fixed at $V_{dd} = 0$ V. The resulting tuning curves under both lighting extremes are shown in Fig 5(b). It can be seen that the attenuator achieves a dynamic-tuning range of more than 25 dB at the center frequency of 38 GHz. The resulting bias-dependent measurement-error characteristic is also shown in Fig. 5(b). It can seen that there is a main error peak located at approximately 0.2 V and an unexpected linearly increasing error above pinchoff. With the main error peak, the external photovoltaic effect only applies to the active biphase modulator since the gate bias resistors of the deactivated modulator are effectively open circuit. Therefore, at zero bias and while illuminated, the voltage reflection coefficient of the reflection termination impedance associated with the active modulator develops a larger magnitude (since it now has a lower drain–source channel resistance) compared to the reflection coefficient associated with the deactivated modulator. This results in a 3-dB reduction in the level of insertion loss. With the linearly increasing error and with no illumination, as the negative-gate bias potential is increased above pinchoff, the corresponding reduction in the value of Cgs, results in an increasing deviation in the phase angle of the active modulator's reflection coefficient. Therefore, the signals emerging from both arms of the balanced topology may still be of equal magnitude, but are now no longer in-phase—resulting in an increase in the level of insertion loss. However, when illuminated, Cgs is increased and the phase angle deviation is minimized. The worst-case error of almost 3 dB in the expected level of insertion loss could have noticeable consequences.

Because the drain–source channel resistance is inversely proportional to the FET's peripheral size, the location of the error peaks will be at lower values of negative-gate bias potentials if smaller transistors are employed and, conversely, at higher potentials if larger transistors are employed. Moreover, unlike variable-gain amplifiers, the location of the peaks will not, in general, depend on the design frequency of operation, as the size of the devices are generally not frequency scaled—if the effects of the unwanted parasitic elements are ignored. However, as with variable-gain amplifiers, the size of the error
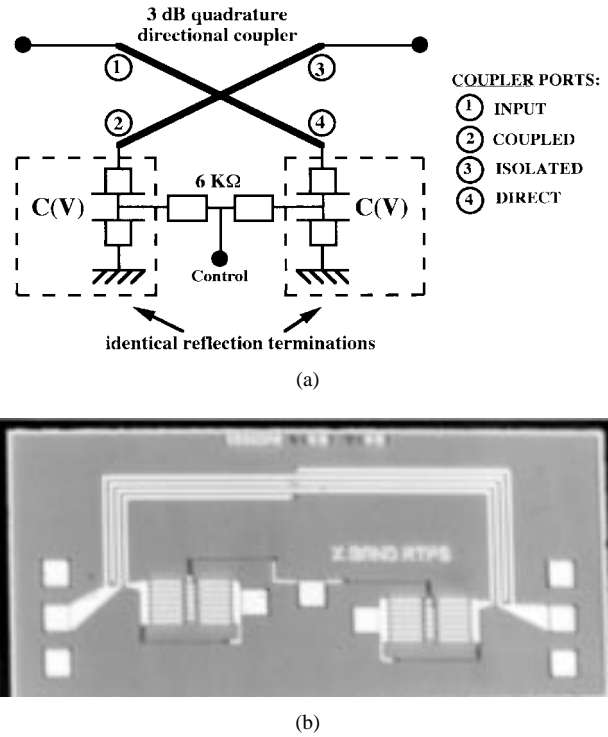

(a)

(b)

Fig. 6.   Microwave analog phase shifter. (a) Topology. (b) Microphotograph.

peaks will again depend on the FET technology used and be proportional to the FET's peripheral size.

VI. ANALOG PHASE SHIFTERS

As with variable-gain blocks, variable-phase blocks are used extensively in general microwave signal-processing applications [1], [4], [21], [27]. The analog reflection-type phase shifter (RTPS) can come in at least four generic wide-band versions [1]:

1) two-stage "cascaded-match" version, which has no bias-dependent group-delay variation [27]–[30];
2) single-stage "maximum relative phase shift" version, which has a small level of bias-dependent group-delay variation [3];
3) single-stage "minimum group-delay variation" version, which has a reduced level of maximum relative phase shift [3];
4) single-stage "analog delay line" version, which has a large linear bias-dependent group-delay variation [3].

The results of a preliminary investigation into the effects of photonic absorption on the "cascaded-match" RTPS has been previously documented [30].

A. MESFET-Based Phase Shifter

In this section, the single-stage "maximum relative phase shift" RTPS is considered, with its topology shown in Fig. 6(a). This reflection topology consists of a 3-dB quadrature directional coupler with identical MESFET varactors that act as voltage-controlled variable-reactance reflection terminations. As with the attenuator, because of the inherent characteristics of the directional coupler, this

reflection topology can be effectively treated as a single-MESFET circuit. As the reverse-bias potential increases, the junction capacitance decreases and, therefore, the capacitive reactance increases. As a result, the insertion phase of the network advances, causing an increase in phase shift, relative to the reference level of insertion phase.

Interdigitated planar Schottky varactor diodes (IPSVD's) implemented using F20 MESFET's have been accurately characterized up to 40 GHz [30]–[33] and subsequently deployed in numerous applications, ranging from phase shifters for adaptive microwave signal-processing applications [3], [27], [29] to voltage-controlled oscillators (VCO's) [34] to highly selective tunable active bandpass filters [24] and tunable notch filters [25]. A conventional HEMT varactor has also been accurately characterized at microwave frequencies [35]. The resulting model demonstrated a tuning behavior, which is very similar to that found with the F20 MESFET varactor.

A microphotograph of the MMIC phase shifter is shown in Fig. 6(b) [3]. Each reflection termination employs two 900-μm MESFET varactors in a back-to-back arrangement (for doubling the maximum level of RF power). Tuning is achieved by simply varying the anode voltage. The tuning curve while illuminated, with the reference insertion phase taken under the same lighting condition and at a forward bias potential of +0.5 V, is shown in Fig. 7(a). In addition, the tuning curve with no illumination, but with the reference insertion phase taken while illuminated, is also shown in Fig. 7(a). This scenario emulates the worst-case condition, where the phase shifter is calibrated while illuminated and subsequently packaged. It can be seen that the phase shifter achieves a maximum relative phase shift of 100° at the center frequency of 10 GHz.

With illuminated MESFET varactors, the Schottky-junction capacitance increases and the overall series resistance decreases due to both the photoconductive and photovoltaic effects. The bias-dependent measurement-error characteristic (i.e., the difference in the relative phase-shift responses) is shown in Fig 7(a). It can be seen that a 9.2° error peak is located just above the point-of-inflection in the tuning curve (at 1.20 V). When deployed as a single-stage analog phase shifter, an increase of 9.2° in the expected level of relative phase shift could have dramatic consequences when integrated into a system.

With MESFET varactors implemented using GMMT's F20 process, the n$^+$ capping layer extends right up to the anode (gate) electrode, as illustrated in Fig. 1(a). As a result of having such a short access region when the reverse bias voltage is increased, the lateral depletion is more dominant than the vertical depletion [33]. The point-of-inflection is believed to correspond to the point at which lateral depletion reaches the cathode (drain and source) electrodes. With MESFET varactors that have significantly longer access regions, vertical depletion is more dominant, giving a point-of-inflection near pinchoff [36].

B. pHEMT-Based Phase Shifter

In this section, two identical single-stage "*minimum group-delay variation*" RTPS's are cascaded in order to increase the
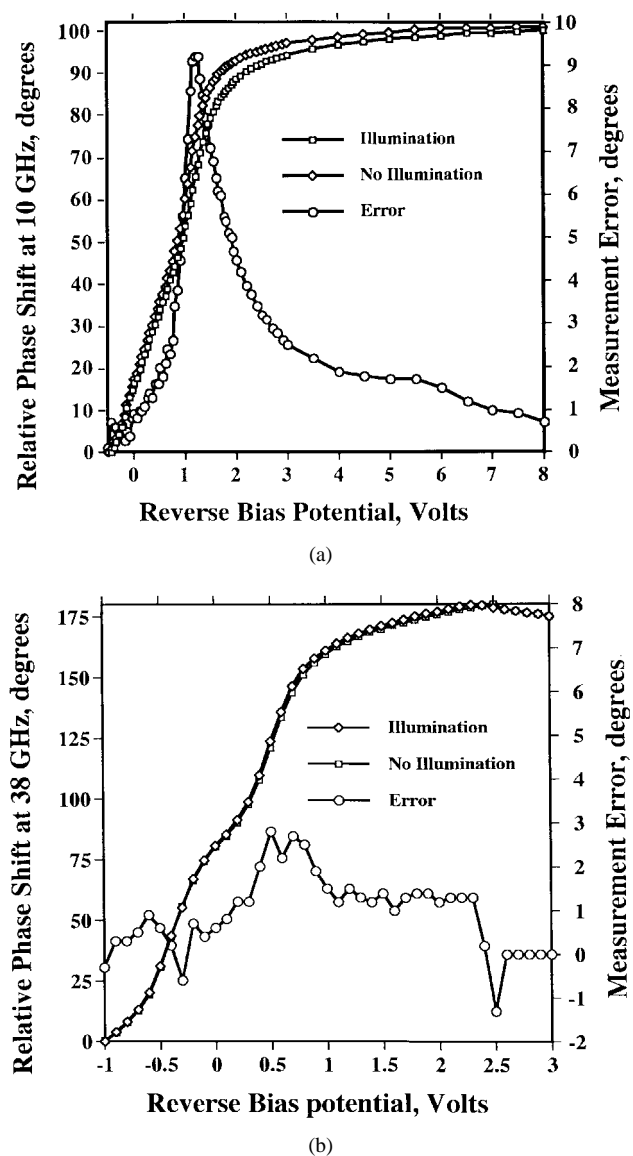

Fig. 7. Measured anomalous optical behavior for the analog phase shifter. (a) MESFET circuit. (b) pHEMT circuit.

maximum level of relative phase shift. Here, the topology of each stage is similar to the microwave phase shifter (but with a 375-Ω anode bias resistor), except that each reflection termination employs two 80-μm pHEMT varactors in a back-to-back arrangement and an additional series inductance.

The tuning curve while illuminated along with the reference insertion phase taken under the same lighting condition and at a forward bias potential of +1.0 V is shown in Fig. 7(b). In addition, the tuning curve with no illumination, but with the reference insertion phase taken while illuminated, is also shown in Fig. 7(b). It can be seen that the phase shifter achieves a maximum level of relative phase shift of 176° at the center frequency of 38 GHz.

It can be seen that there are two small error humps with the pHEMT-based phase shifter. These correspond to two points-of-inflection in the tuning curves. The first hump, at a forward bias of +0.6 V, has a value below 1.0°, while the second peak, at a reverse bias of +0.6 V, has a value of 2.8°. For many

applications, the worst-case increase of 2.8° in the expected level of relative phase shift would not have a significant effect on a system's performance.

With pHEMT varactors implemented using GMMT's H40 process, the n^+ capping layer extends right up to the anode electrode, as illustrated in Fig. 1(b). The first point-of-inflection is believed to correspond to the point at which vertical depletion reaches the 2-D electron gas, while the second point-of-inflection corresponds to the point at which lateral depletion reaches the source electrode.

It has been found that error peaks will always be located at the same bias potential, for the same FET technology, and the same generic version of RTPS, irrespective of the frequency of operation. This is because the optimal values for all of the components used have been determined empirically and should, therefore, be directly scaled to the center frequency of operation. With respect to the location of the error peak, the important differences between the generic RTPS's are the values of series inductance and maximum capacitance in the reflection terminations [1]. Previously, it has been found that the F20 MESFET-based "*cascaded-match*" RTPS, which employs relatively high values of series inductances, has an error peak at 1.65 V [30]. While the F20 MESFET-based "*maximum relative phase-shift*" RTPS, having no series inductance, has an error peak at 1.20 V. Also, the size of the error peak will depend on the FET technology used and be proportional to the FET's peripheral size. Therefore, since the size of the IPSVD's are inversely proportional to frequency, the error peaks will be smaller at higher frequencies of operation.

Finally, it was previously found that the MESFET-based "*cascaded-match*" RTPS also exhibits a bias-dependent measurement-error peak in the insertion-loss performance [30]. However, the worst-case error is only of the order of 0.1 dB. This is because of the F20 MESFET's short-gate access region [33], common with that of the H40 pHEMT. Therefore, with the F20 and H40 processes, the measurement anomalies associated with insertion loss are not considered significant for this or any of the other generic version of RTPS fabricated at GMMT. In contrast, with an IPSVD implemented with an FET having a significantly longer access region, a large peak in the series resistance and sudden drop in junction capacitance are observed at pinchoff [36] and, therefore, very large error peaks can be expected in this region.

VII. DISCUSSION

For the three different circuit functions, the levels of sensitivity (defined here as the ratio of peak measurement error normalized to the maximum dynamic-tuning range) can be attributed to: 1) the FET technology; 2) the FET's mode of operation; and 3) the topology of the circuit. With all three functions, there are significant reductions in the optical sensitivity when replacing the MESFET's in the microwave circuits with the pHEMT's in the corresponding millimeter-wave circuits.

There are a number or reasons why the F20 MESFET-based circuits are more sensitive than the corresponding H40

pHEMT-based circuits. The first and most obvious reason is that the peripheral size of the pHEMT's used in the amplifier, attenuator, and phase shifter are reduced to 30%, 40%, and 9%, respectively, from the original MESFET size. Secondly, very large gate bias resistors were employed with the MESFET-based circuits; thus, considerably magnifying the influence of the external photovoltaic effect. The third reason can be visibly seen in Fig. 1, which illustrates the relative lateral dimensions associated with the gate regions of the MESFET's and pHEMT's. Compared to the MESFET, the pHEMT has a 70% reduction in the amount of the exposed active semiconductor area (between the source and drain electrodes). The fourth and more subtle reason is that the number of photo-induced electron–hole pairs generated in a hot pHEMT's supply layer will be insignificant, compared to the number of carriers already supplied by this highly doped layer. In contrast, the number of electron–hole pairs generated in the MESFET's channel, which has a level of doping concentration reduced by one order of magnitude, is proportionally significant. The fifth reason is that, compared to the pHEMT, more thermally induced electron–hole pairs will be generated within the MESFET due to the increase in thermal impedance between the channel and backface metallization layer (since the substrate thickness of the MESFET is twice that of the pHEMT). This will help maintain higher temperatures in the MESFET's active layer. Since the halogen bulb is remote from the MMIC-under-test, there is no direct contribution from the light source. Instead, there may be a noticeable effect when operating a hot FET close to its drain–source current saturation level—as found with a Class-A amplifier designed for maximum power gain. Lastly, the problems associated with the photoconductive effect can be extended to the mesa-etched resistors (which are isolated regions of doped semiconductor having ohmic contacts at both ends) used in the F20 process; since the H40 process employs nichrome resistors. When illuminating a mesa-etched resistor having a relatively large surface area, the resulting drop in resistance could be significant and, therefore, could have dramatic consequences if employed in a sensitive biasing network or feedback network. Moreover, when implementing a high-value gate bias resistor, even a small photocurrent generated within the resistor can induce a significant photovoltage, which will reduce the level of reverse gate bias.

In contrast, there is at least one reason why the MESFET-based circuits could demonstrate less sensitivity than would otherwise be expected, compared to the corresponding pHEMT-based circuits. Unlike the F20 ion-implanted MESFET's, the H40 epitaxially grown pHEMT's could, in principle, suffer from internal photovoltaic effects. However, because the pHEMT has superior carrier confinement, which is well away from the interfacial depletion region, the effects of any back-gating will not be noticeable.

VIII. CONCLUSIONS

From an extensive experimental study, it was found that under ambient laboratory lighting conditions the different voltage-tunable analog-control MMIC's did not suffer from measurement anomalies. However, it has been demonstrated

that these practical control MMIC's can be susceptible to measurement anomalies due to photonic absorption when illuminated under conventional optical microscope lighting conditions.

Prominent error peaks were found at bias points unique to the three different circuit topologies. With the variable-gain amplifier, the peak is always located at the pinchoff voltage. However, with the analog attenuator, peaks are located at gate potentials that cause the channel resistance to equal 50 Ω, with no illumination and when illuminated. With the analog phase shifter, peaks are located at potentials associated with points-of-inflection on the tuning curves.

If there is an increase in either the level of optical illumination, the peripheral size of the FET, or the value of gate bias resistance, then any error peaks will also increase in size, with the three circuit topologies considered here. Large error peaks were found with the MESFET-based microwave circuits. However, with the subsequent change in FET technology, the reduction in the FET's peripheral size and the use of low-value nichrome bias resistors, it has been shown that the pHEMT-based millimeter-wave circuits can be considerably less susceptible to measurement anomalies due to photonic absorption.

If multiple stages are cascaded in order to increase dynamic-tuning range, error peaks will increase dramatically in size. On the other hand, with the appropriate level of optical illumination and/or value of gate bias resistance, this scenario could then be exploited to provide intentional optical control, as demonstrated by many researchers. For example, on inspection of the measured data for all the MESFET-based MMIC's, its has been found that the value of gate photovoltage is $V_{\rm ph} \approx 0.1$ V. With the external bias resistance of $R_b = 6$ kΩ, the gate's photocurrent is $I_{\rm ph} \approx 16.7$ μA. Therefore, under the same level of optical illumination, a cold MESFET can be optically switched from the "off" state to the "on" state with a new gate bias resistance of $R_b = V_{\rm pinchoff}/I_{\rm ph} \approx 120$ kΩ.

The MMIC's discussed in this paper have all been simple voltage-tunable analog-control circuits. However, if a MMIC employs a number of FET devices, even in a slightly more complex topology (e.g., a VCO or tunable active filter), the anomalous optical behavior of the circuit may not be so easily understood.

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Stepan Lucyszyn (M'91) was born in Bradford, U.K., in 1965. He received the B.Sc. degree in electronic and communication engineering from the Polytechnic of North London, London, U.K., in 1987, the M.Sc. degree in satellite communication engineering from the University of Surrey, Surrey, U.K., in 1988, and the Ph.D. degree from King's College London, London, U.K., in 1992, for his work on ultra-wide-band phase shifters for MMIC applications.

In 1989, he worked in the British and French space industries, as a Junior Consultant on a broad range of projects. From 1992 to July 1995, he worked as a Post-Doctoral Research Fellow at King's College London. Since August 1995, he has been on the academic staff as Lecturer in RF Electronics at the University of Surrey. He has co-authored approximately 50 research papers in the broad area of microwave and millimeter-wave engineering for both national and international conferences and journals. In addition, he contributed three chapters to *MMIC Design*, (London, U.K.: IEE, 1995). He is on the editorial board for the *International Journal of Electronics*.

Dr. Lucyszyn is a Chartered Engineer, U.K. (since 1993). He serves on the IEE Professional Group Committee E12 (Microwave Devices and Techniques). He is a member of the EPSRC Peer Review College 9 (Electronics and Photonics), serves on the editorial boards for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and is a referee for *IEE Electronics Letters*.

Ian D. Robertson was born in London, U.K., in 1963. He received the B.Sc. and Ph.D. degrees from King's College, University of London, London, U.K., in 1984 and 1990, respectively.

From 1984 to 1986, he was with the MMIC Research Group, Plessey Research, Caswell, U.K., where he worked on MMIC mixers, on-wafer measurement techniques, and FET characterization. From 1986 to 1998, he was with King's College, first as a Research Assistant, and then as a Lecturer and Reader in microwave engineering. In 1998, he took up the Chair of Microwave Subsystems Engineering, University of Surrey, Surrey, U.K., where he currently leads an active research group in RF, microwave, and millimeter-wave circuit design and applications engineering. His research interests encompass all aspects of the design and application of MMIC's. He edited *MMIC Design* (London, U.K.: IEE, 1995).